



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/890,376	02/21/2002	Jorg Horzel	0522-1752	2008

7590

05/24/2004

William M Lee Jr
Lee Mann Smith McWilliams Sweeney & Ohlson
PO Box 2786
Chicago, IL 60690-2786

EXAMINER

SCHILLINGER, LAURA M

ART UNIT

PAPER NUMBER

2813

DATE MAILED: 05/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/890,376

Applicant(s)

HORZEL ET AL

Examiner

Laura M Schillinger

Art Unit

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 9 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 19-33 is/are pending in the application.
- 4a) Of the above claim(s) 34 and 35 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 19-33 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2/21/02
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

Applicant's election of claims 19-33 in Paper dated 4/9/04 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claims 34-35 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected claims, there being no allowable generic or linking claim. Election was made **without** traverse in Paper dated 4/9/04.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 19-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Tayanaka

(213).

Art Unit: 2813

19. Tayanaka teaches a method for fabricating a solar cell on a reusable substrate of a semiconductor material comprising the steps of:
providing a substrate of a semiconductor material having at least one surface (Fig. 25 (11));
forming at least one porous layer on said surface of said substrate (Fig. 25D (12M));
depositing at least one semiconductor layer on said porous layer (Fig. 25D (101));
forming active devices in said semiconductor layer including forming at least one n-type doped region and at least one p-type doped region in said semiconductor layer of each active device, said n-type and p-type regions having an exposed surface (Col. 35, lines: 5-15),
forming electrical contacts to said active devices including forming metal contacts to the exposed surfaces of said n-type region and said p-type region of said active devices (Fig. 26A (102)),
attaching a support to the surface overlying said metal connections (Fig. 26C (104)), and
non-mechanically detaching said substrate from said semiconductor layer by removing said porous layer with a wet chemical etch using said support as an etch mask (Col. 9, lines: 55-61 and Col. 35, lines: 30-35).

20. Tayanaka teaches a method as recited in claim 19, wherein said porous layer on said surface of said substrate is formed by an electroless etching technique in an aqueous chemical solution (Col. 35, lines: 30-35).

21. Tayanaka teaches a method as recited in claim 19, wherein said surface of said substrate is textured or structured prior to forming said porous semiconductor layer (Col. 2, lines: 25-35).

Art Unit: 2813

22. Tayanaka teaches a method as recited in claim 19, wherein said support is a flexible sheet material (Col.33, lines: 50-55).
23. Tayanaka teaches a method according to claim 19, wherein said support is composed of a plastic or a polymer (Col.7, lines: 5-15).
24. Tayanaka teaches a method according to claim 19, wherein said porous layer is a single porous semiconductor layer (Fig.25D (12M)).
25. Tayanaka teaches a method as recited in claim 24, wherein said single porous semiconductor layer is formed such that there is a gradient in porosity (Fig.23 and 24).
26. Tayanaka teaches a method as recited in claim 24, wherein said porous semiconductor layer is a porous silicon layer, said method further comprising the step of thermally oxidizing said porous silicon layer to thereby convert said porous silicon layer to a porous silicon oxide layer (Col.10, lines: 54-60).
27. Tayanaka teaches a method as recited in claim 26, wherein said substrate is detached from said semiconductor layer by removing said porous silicon oxide layer using a wet chemical etch, said wet chemical etch being selective to said substrate and said semiconductor layer (Col.9, lines: 55-61 and Col.35, lines: 30-35).

28. Tayanaka teaches a method as recited in claim 19, wherein said metal contacts are formed by screen printing a first metal paste to contact said p-type doped regions and a second metal paste to contact said n-type doped regions (Col.14, lines: 1-5).
29. Tayanaka teaches a method according to claim 19, wherein said semiconductor material of said substrate is selected from the group consisting of Si, SiGe, Ge, GaAs (Col.12, lines: 45-60).
30. Tayanaka teaches a method as recited in claim 29, wherein said substrate is doped with either an n- type impurity or a p-type impurity, said substrate having a highly doped surface region whereon said porous layer will be formed (Col.34, lines: 15-20).
31. Tayanaka teaches a method according to claim 19, wherein each of said semiconductor layers is either an n-type or a p-type doped layer being composed of a semiconductor material selected from the group consisting of Si, (Col.27, lines: 50-60)
32. Tayanaka teaches a method as recited in claim 31, wherein said thin film semiconductor devices are thin film solar cells having a plurality of actively collecting semiconductor layers of different doping types (Col.1, lines: 20-45).
33. Tayanaka teaches a method according to claim 19, wherein after detaching said substrate an additional layer is formed on exposed pads of said semiconductor layer, said additional layer

Art Unit: 2813

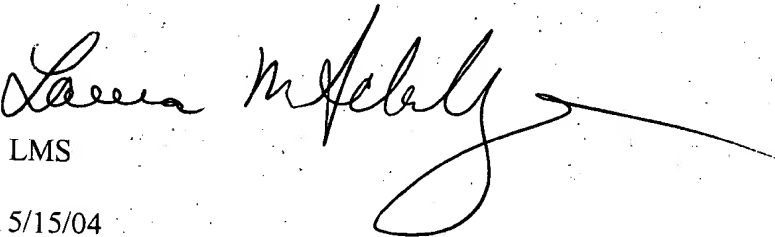
being used at least as a passivation layer or an anti-reflective coating layer or a back surface reflector layer (Col. 14, lines: 1-10).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M Schillinger whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


LMS

5/15/04